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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,237	07/29/2003	Makoto Shizukuishi	107317-00060	4755

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ARENT FOX KINTNER PLOTKIN & KAHN, PLLC  
Suite 400  
1050 Connecticut Avenue, N.W.  
Washington, DC 20036-5339

EXAMINER
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TRAN, NHAN T

ART UNIT	PAPER NUMBER
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2622

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07/20/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/628,237	SHIZUKUISHI, MAKOTO	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 April 2007 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

## DETAILED ACTION

### *Response to Arguments*

1. Applicant's arguments filed 4/30/2007 have been fully considered but they are not persuasive.

The Applicant asserts that Morris in view of Tran does not teach the limitations as amended in claim 1 that includes "*a number of photoelectric conversion elements disposed in a light receiving area of a semiconductor substrate in a matrix shape and in a first number of rows and a second number of columns; analog digital converters, each formed for each column of the photoelectric conversion elements in an area of the semiconductor substrate other than the light receiving area, the analog digital converters converting analog image data from the photoelectric conversion elements into digital image data; and a non-volatile memory formed in an area of the semiconductor substrate other than the light receiving area at a succeeding stage of the analog digital converters, the non-volatile memory having memory units, each corresponding to one of the photoelectric conversion elements, and recording the digital image data.*" (Remarks, pages 8-11).

In response, the Examiner understands the Applicant's arguments but respectfully disagrees with the Applicant's assessment of the claim.

In Morris, a two-dimensional image sensor (104) is disclosed (Fig. 1). It is clear in Morris that the image sensor (104) comprises rows and columns of pixels, each addressed by row shift register (108) and column shift register (112), respectively, in a

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matrix shape (see Fig. 1 and col. 2, lines 16-33). Regardless of arranging in blocks of 8 x 64 pixels, the total number of pixels in eight blocks (64 x 64) is arranged within the matrix shape having rows and columns in conventional fashion as disclosed. Morris clearly discloses an array of analog to digital converters (ADC array 120) each formed for each column of the photoelectric conversion elements in an area of the semiconductor substrate other than the light receiving area (Fig. 1; col. 1, lines 39-46 and col. 2, lines 53-65). Furthermore, Morris discloses a memory array (130) formed in an area of semiconductor substrate other than the light receiving area at a succeeding stage of the analog to digital converters (see Fig. 1). It is also seen in Morris that each memory block comprises 8 x 128 bit-memory and the total memory size is 64 x 128 bits. Such the memory size is fully capable of storing the whole image frame comprising 64 x 64 pixel array, and therefore, each memory unit (memory cell) is corresponding to one of the photoelectric conversion elements (pixels) for recording the digital image data (see col. 3, lines 3-10).

Although Morris does not teach that the memory array (130) is a non-volatile memory, this lack of teaching is compensated by Tran as addressed in the previous office action.

In view of the above, the rejection of claims 1-16 is maintained. New claim 17 is also rejected as set forth below.

### ***Drawings***

2. The drawings filed 4/30/2007 to include "Prior Art" legend for Fig. 9 are accepted.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 7, 8, 14 & 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of claims 7, 8, 14 & 15 recites the limitation "said signal processor(s)."

There is insufficient antecedent basis for this limitation in the claims.

*Note: the following art rejection applied to claims 7, 8, 14 and 15 are based on best understood in view of the 35 USC 112 above.*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 17 & 18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claims contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

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Regarding claim 17, although specification discloses horizontal data register (4) for registering (buffering) image data output from the A/D converter (3) and/or the non-volatile memory units (6) (see entire specification), **no where** in the specification discloses horizontal address decoder which decodes horizontal address of **both** the photoelectric conversion elements and the non-volatile memory units. At best seen from the disclosure, the horizontal data register (4) might decode address for the memory units but **not** for the photoelectric conversion elements because the horizontal data register (4) is simply not disclosed as a horizontal address decoder for the photoelectric conversion elements. Instead, it is implemented for registering (buffering) image data output from the A/D convert (3) and outputting the image data to an output port but not for address decoding function for the photoelectric conversion elements.

Regarding claim 18, this claim is dependent from claim 17.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-8, 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. (US 6,573,936 B2) in view of Tran et al. (US 6,282,145 B1).

Regarding claim 1, Morris et al. (hereafter referred as "Morris") discloses a solid state image pickup device (Fig. 1; col. 1, lines 39-46 and col. 2, lines 16-33) comprising:

a semiconductor substrate (chip substrate) defining a two-dimensional surface (Fig. 1 and col. 1, lines 39-46 and col. 2, lines 10-16);

a number of photoelectric conversion elements (pixel sensors) disposed in a light receiving area (pixel array area 104 shown in Fig. 1) of said semiconductor substrate in a matrix shape (two dimensional matrix shape) and in a first number of rows and a second number of columns (see col. 2, lines 16-33);

analog digital converters (array of A/D converters 120 shown in Fig. 1), each formed for each column of said photoelectric conversion elements in an area (area 120) of said semiconductor substrate other than the light receiving area (Fig. 1 and col. 2, lines 53-58), said analog digital converters converting analog image data from said photoelectric conversion elements into digital image data (see col. 2, lines 53-65);

a memory (memory array 130) in an area of said semiconductor substrate other than the light receiving area at a succeeding stage of analog digital converters (Fig. 1), said memory having memory units (memory cells), each corresponding to of the photoelectric conversion elements, and recording the digital image data (see col. 1, lines 39-46 and col. 3, lines 3-10, note the Examiner's response in section 1 above).

Morris teaches that the memory (130) is a random access memory (RAM), etc. (col. 3, lines 8-10), and fails to teach that the memory is a non-volatile memory.

In the same field of endeavor for processing and storing image signals in an image pickup apparatus, Tran et al. (hereafter referred as "Tran") teaches a memory

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improvement for storing digital images (Fig. 1D) by using a non-volatile memory (2000) to replace a conventional random access memory (RAM) because the non-volatile memory retains image data in memory cells even if the power supply is removed. This is contrast to volatile memory (RAM) which loses data if the power supply is removed (see Tran, col. 1, lines 22-35). Tran further teaches that the non-volatile memory is also preferred due to its small size with a high density array for an integrated single chip camera (integrated circuit ECAM 2005 shown in Fig. 1D) comprising an image sensor (2003), A/D converter (2002), non-volatile memory (2000) and a microcontroller (2001) (see Tran, col. 1, lines 36-41 and col. 6, lines 34-58).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the image pickup device in Morris to use a non-volatile memory array in place of memory array 130 within the single chip image pickup device in view of the teaching of Tran so that image data is retained in the memory cells even if power supply is removed from the device (by accident or other causes) so as to prevent lost of image data during image capturing process.

Regarding claim 2, the combined teachings of Morris and Tran also discloses that the non-volatile memory records the digital image data of one frame (see Tran, col. col. 2, lines 7-17 in which the non-volatile memory has a capacity of giga bits that are inherently capable of recording one or more image frames).

Regarding claim 3, the limitations are also met by the analysis of claim 2 in which the non-volatile memory records the digital image data of a plurality of frames.

Regarding claim 4, the combined teachings of Morris and Tran also discloses erasing means (memory controller 132, 134 in Morris) for erasing the digital image data after the digital image data stored in said non-volatile memory (modified memory 130 in claim 1) is read to an external (via I/O interface 160 in Morris). See Morris, Fig. 1, col. 3, lines 10-12 & col. 7, lines 20-30 and Tran, col. 4, lines 50-54 and col. 6, lines 53-56. It should be noted that since the non-volatile memory is on-chip memory, in order to capture more new images when the memory is full with previously captured images, the previous images stored in the memory must be erased by memory controller either automatically or manually after the images are transferred to an external device via I/O interface to yield memory space for capturing the next images for the single chip image pickup device to function as disclosed.

Regarding claim 5, Morris in view of Tran as analyzed in claim 1 also teaches that addresses of said non-volatile memory (modified memory 130 in claim 1) in a vertical direction are related to addresses of the light receiving area in the vertical direction (see Morris, Fig. 1 in which the addresses of memory 130 and pixel array 104 in a vertical direction are related in order to perform parallel processing as disclosed in col. 3, lines 3-10 and col. 7, lines 20-30).

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Regarding claim 6, Morris in view of Tran as analyzed in claim 1 discloses a data register (latch B shown in Fig. 4 of Morris) used in common for both data input and output for said non-volatile memory (modified memory 130; see Morris, col. 4, lines 46-55, wherein latch B is used as data register for both reading from and writing to memory 130).

Regarding claim 7, Morris in view of Tran as analyzed in claim 1 also teaches that said non-volatile memory (modified memory 130) has a depth of same bits (8 bits) as output bits (8 bits) of said analog digital converter (120) provided for each column. See Morris, col. 3, lines 3-8 & col. 2, lines 53-58 and Tran, col. 7, lines 31-36.

Regarding claim 8, Morris in view of Tran as analyzed in claim 1 discloses that each of said analog digital converters (each of A/D converters 120) outputs the digital image data of one row of said photoelectric conversion elements in parallel, and said non-volatile memory (modified memory 130) records the digital image data of one row output parallel at a memory position corresponding to a row direction (array of memory 130 is arranged in a row direction to receive digital image data row by row output from the A/D converter array 120 in parallel fashion for parallel processing as disclosed by Morris, Fig. 1, col. 1, lines 10-14 and col. 3, lines 3-10).

Regarding claim 15, Morris further discloses a MOS circuit (an inherent MOS transistor in the CMOS image array 102) for reading charges from said photoelectric

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conversion elements in the light receiving area and transfers analog image data to said analog digital converter (120) provided for each column, and wiring lines (see Morris, Fig. 1 and col. 2, lines 29-33).

Regarding claim 16, Although Morris discloses that the solid state image pickup device works as a digital camera (Morris, col. 1, lines 39-46), Morris is silent about a shutter control unit and an optical system. However, such lack of teaching is compensated by Tran. Tran clearly teaches an integrated chip as a digital camera system (SILICONCAM 2008 shown in Fig. 1D) includes a shutter control unit (microcontroller 2001 for controlling exposure time which represents a shutter control unit), an optical system (lens block 2004) for focusing an image of an object. See Tran, col. 6, lines 34-58.

Therefore, it would have been obvious to one of ordinary skill in the art to combine teachings of Morris and Tran to arrive at the Applicant's claimed invention by integrating a shutter control unit for controlling exposure time of the image sensor, an optical system for focusing an image of an object into the image sensor in addition to other necessary components to make a single chip digital camera to capture quality digital images while reducing size of the camera.

Regarding claim 14, Morris teaches a CMOS for reading charges from said photoelectric conversion elements in the light receiving area and transfers analog image data to said signal processor provided for each column (see the analysis of claim 15).

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Morris does not teach a CCD for reading charges from the photoelectric conversion elements.

As suggested by Tran, an image sensor (2003) can be either a CMOS circuit or an alternative CCD circuit for reading charges from photoelectric conversion elements (Tran, col. 6, lines 45-46).

Therefore, it would have been obvious to one of ordinary skill in the art to use a CCD in an alternative configuration for reading signal charges from the photoelectric conversion elements since the CCD is known as having an advantage in providing higher dynamic range of image signals than CMOS sensor.

Regarding claim 17, Morris in view of Tran also discloses that positions of said photoelectric conversion elements are identified by horizontal position and vertical position (row and column shift registers 108 & 112 shown in Fig. 1 of Morris), and said non-volatile memory units (modified memory units as discussed in claim 1) are identified by two dimensional addresses (x, y), x and y corresponding, respectively, to the horizontal and vertical positions of the photoelectric conversion element (see Tran, col. 14, lines 22-24, and note that the non-volatile memory is a two-dimensional memory for storing a two-dimensional image data. Thus, x and y addresses in the memory would inherently be corresponding to the horizontal and vertical positions of the pixels in the combination of Morris and Tran).

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6. Claims 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morris et al. and Tran et al. as applied to claim 1 and in further view of Yamazaki et al. (US 6,556,475 B2).

Regarding claims 9 & 10, the combination of Morris and Tran is silent about the non-volatile memory being a NAND type transistor memory (claim 9) or a NOR type transistor memory (claim 10). However, as taught by Yamazaki et al. (hereafter referred as "Yamazaki"), it is well recognized in the art that non-volatile memory can be made with a NAND type transistor memory, a NOR type transistor memory, etc. (Yamazaki, col. 1, lines 40-49). Regardless the types, the non-volatile memory is highly desired for storing data in various electronic devices for substituting volatile memory such as DRAM (Yamazaki, col. 1, lines 32-40).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the non-volatile memory in Morris and Tran with a NAND type transistor memory or an alternative NOR type transistor memory for storing image data in view of the teaching of Yamazaki because both types have a common advantage of retaining image data in memory cells even if the power supply is removed and are highly desirable for storing data in electronic devices while providing more choices and flexibility to designer for making different image pickup models based on different types of transistor memories toward different camera applications and consumers.

Regarding claims 11 & 12, the combination of Morris, Tran and Yamazaki further discloses that the transistor memory has a floating gate type memory structure, MONOS type memory structure (see Yamazaki, col. 1, lines 40-49).

Regarding claim 13, the combination of Morris, Tran and Yamazaki also discloses that the transistor memory is a ferroelectric memory (see Tran, col. 4, lines 30-42).

### ***Conclusion***

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NHAN T. TRAN  
Patent Examiner

A handwritten signature in black ink, appearing to read 'David Ometz', with a long horizontal flourish extending to the right.

DAVID OMETZ  
SUPERVISORY PATENT EXAMINER